

# LH52258A

CMOS 32K × 8 Static RAM

## FEATURES

- Fast Access Times: 20/25 ns
- Low-Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully-Static Operation
- JEDEC Standard Pinout
- Packages:
  - 28-Pin, 300-mil DIP
  - 28-Pin, 300-mil SOJ

## FUNCTIONAL DESCRIPTION

The LH52258A is a high-speed 262,144 bit static RAM organized as 32K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ( $\bar{E}$ ) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power ( $I_{SB1}$ ) drops to its lowest level if  $\bar{E}$  is raised to within 0.2 V of  $V_{CC}$ .

Write cycles occur when both Chip Enable ( $\bar{E}$ ) and Write Enable ( $\bar{W}$ ) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. The proper use of the Output Enable control ( $\bar{G}$ ) can prevent bus contention.

When  $\bar{E}$  is LOW and  $\bar{W}$  is HIGH, a static Read will occur at the memory location specified by the address lines.  $\bar{G}$  must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

## PIN CONNECTIONS

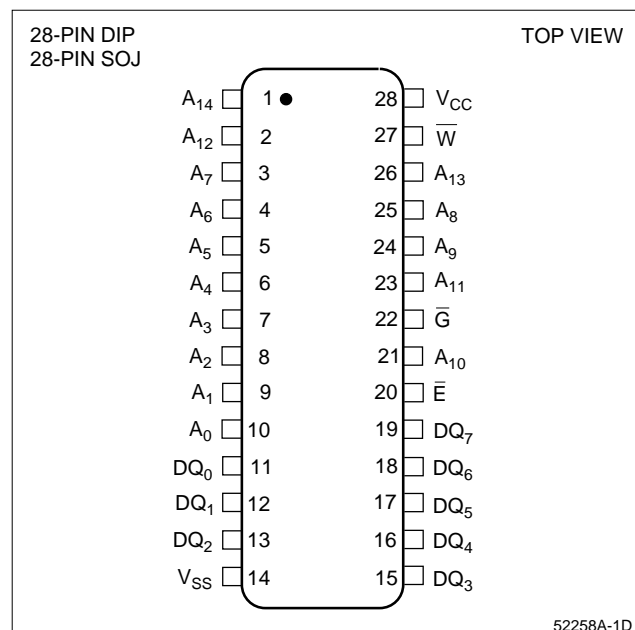
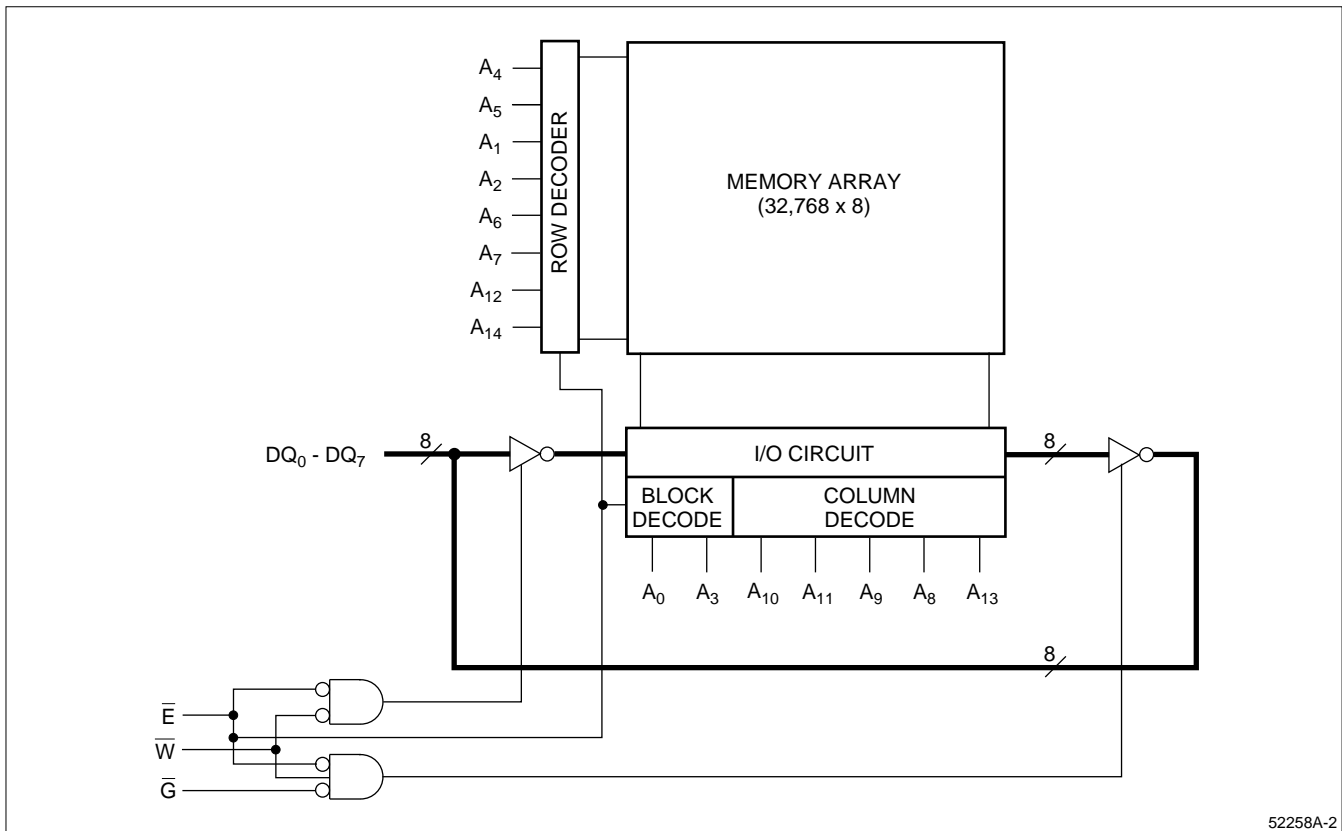


Figure 1. Pin Connections for DIP and SOJ Packages



52258A-2

Figure 2. LH52258A Block Diagram

**TRUTH TABLE**

$\bar{E}$	$\bar{G}$	$\bar{W}$	MODE	DQ	$I_{cc}$
H	X	X	Not Selected	High-Z	Standby
L	H	H	Selected	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

**PIN DESCRIPTIONS**

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
$\bar{W}$	Write Enable
$V_{cc}$	Positive Power Supply
$V_{ss}$	Ground

**ABSOLUTE MAXIMUM RATINGS**<sup>1</sup>

PARAMETER	RATING
V <sub>CC</sub> to V <sub>SS</sub> Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V <sub>CC</sub> + 0.5 V
DC Output Current <sup>2</sup>	± 40 mA
Storage Temperature Range	−65° to 150°C
Power Dissipation (Package Limit)	1.0 W

**NOTES:**

- Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

**OPERATING RANGES**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T <sub>A</sub>	Temperature, Ambient	0		70	°C
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V
V <sub>IL</sub>	Logic '0' Input Voltage <sup>1</sup>	−0.5		0.8	V
V <sub>IH</sub>	Logic '1' Input Voltage	2.2		V <sub>CC</sub> + 0.5	V

**NOTE:**

- Negative undershoot of up to 3.0 V is permitted once per cycle.

**DC ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>1</sup>	MAX	UNIT
I <sub>CC1</sub>	Operating Current <sup>2</sup>	t <sub>RC</sub> = 20 ns G̅ ≥ V <sub>IH</sub> , E̅ ≤ V <sub>IL</sub> , I <sub>OUT</sub> = 0 mA, t <sub>CYCLE</sub> = 20 ns		95	150	mA
I <sub>CC1</sub>	Operating Current <sup>2</sup>	t <sub>RC</sub> = 25 ns G̅ ≥ V <sub>IH</sub> , E̅ ≤ V <sub>IL</sub> , I <sub>OUT</sub> = 0 mA, t <sub>CYCLE</sub> = 25 ns		90	140	mA
I <sub>SB1</sub>	Standby Current	E̅ ≥ V <sub>CC</sub> − 0.2 V		0.005	1	mA
I <sub>SB2</sub>	Standby Current	E̅ ≥ V <sub>IH</sub>		6	15	mA
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V to V <sub>CC</sub>	−2		2	μA
I <sub>LO</sub>	I/O Leakage Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V to V <sub>CC</sub>	−2		2	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = −4.0 mA	2.4			V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8.0 mA			0.4	V
V <sub>DR</sub>	Data Retention Voltage	E̅ ≥ V <sub>CC</sub> − 0.2 V	2		5.5	V
I <sub>DR</sub>	Data Retention Current	V <sub>CC</sub> = 3 V, E̅ ≥ V <sub>CC</sub> − 0.2 V			250	μA

**NOTES:**

- Typical values at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.
- I<sub>CC</sub> is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

### AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V <sub>SS</sub> to 3 V
Input Rise and Fall Times	3 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

### CAPACITANCE <sup>1,2</sup>

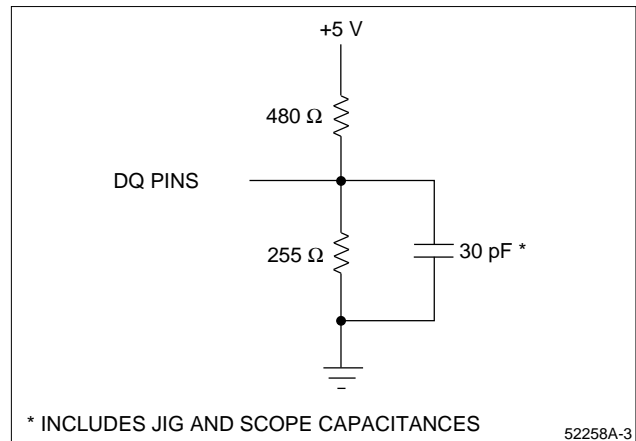
PARAMETER	RATING
C <sub>IN</sub> (Input Capacitance)	7 pF
C <sub>DO</sub> (I/O Capacitance)	8 pF

**NOTES:**

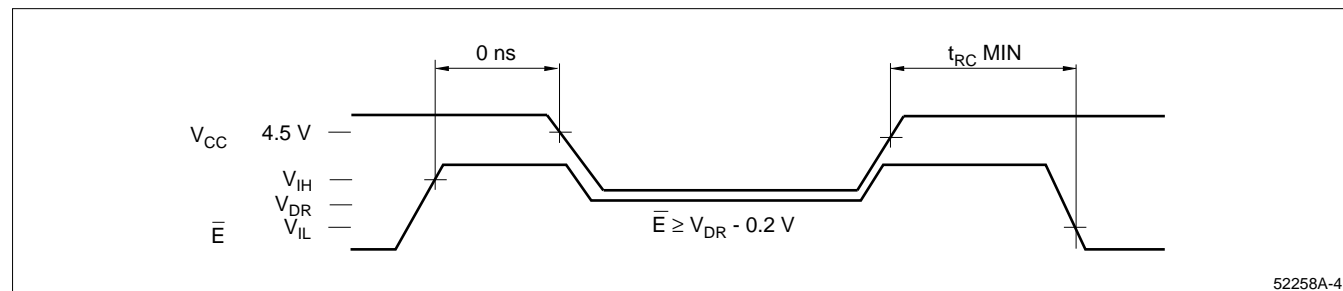
1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V<sub>Bias</sub> = 0 V and V<sub>CC</sub> = 5.0 V.
2. Guaranteed but not tested.

### DATA RETENTION TIMING

$\bar{E}$  must be held above the lesser of V<sub>IH</sub> or V<sub>CC</sub> - 0.2 V to prevent improper operation when V<sub>CC</sub> < 4.5 V.  $\bar{E}$  must be V<sub>CC</sub> - 0.2 V or greater to meet I<sub>DR</sub> specification. All other inputs are 'Don't Care.'



**Figure 3. Output Load Circuit**



**Figure 4. Data Retention Timing**

AC ELECTRICAL CHARACTERISTICS <sup>1</sup> (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		UNITS
		MIN	MAX	MIN	MAX	
<b>READ CYCLE</b>						
t <sub>RC</sub>	Read Cycle Time	20		25		ns
t <sub>AA</sub>	Address Access Time		20		25	ns
t <sub>OH</sub>	Output Hold from Address Change	4		4		ns
t <sub>EA</sub>	$\bar{E}$ Low to Valid Data		20		25	ns
t <sub>ELZ</sub>	$\bar{E}$ Low to Output Active <sup>2,3</sup>	4		4		ns
t <sub>EHZ</sub>	$\bar{E}$ High to Output High-Z <sup>2,3</sup>	0	10	0	12	ns
t <sub>GA</sub>	$\bar{G}$ Low to Valid Data		10		12	ns
t <sub>GLZ</sub>	$\bar{G}$ Low to Output Active <sup>2,3</sup>	0		0		ns
t <sub>GHZ</sub>	$\bar{G}$ High to Output High-Z <sup>2,3</sup>	0	9	0	10	ns
t <sub>PU</sub>	$\bar{E}$ Low to Power Up Time <sup>3</sup>	0		0		ns
t <sub>PD</sub>	$\bar{E}$ High to Power Down Time <sup>3</sup>		25		30	ns
<b>WRITE CYCLE</b>						
t <sub>WC</sub>	Write Cycle Time	20		25		ns
t <sub>EW</sub>	$\bar{E}$ Low to End of Write	15		20		ns
t <sub>AW</sub>	Address Valid to End of Write	15		20		ns
t <sub>AS</sub>	Address Setup	0		0		ns
t <sub>AH</sub>	Address Hold from End of Write	0		0		ns
t <sub>WP</sub>	$\bar{W}$ Pulse Width	12		15		ns
t <sub>DW</sub>	Input Data Setup Time	10		12		ns
t <sub>DH</sub>	Input Data Hold Time	0		0		ns
t <sub>WHZ</sub>	$\bar{W}$ Low to Output High-Z <sup>2,3</sup>		8		10	ns
t <sub>WLZ</sub>	$\bar{W}$ High to Output Active <sup>2,3</sup>	0		0		ns

**NOTES:**

- AC Electrical Characteristics specified at 'AC Test Conditions' levels.
- Active output to High-Z and High-Z to output active tests specified for a  $\pm 500$  mV transition from steady state levels into the test bad. The test load has 5 pF capacitances.
- Guaranteed by design but not tested.

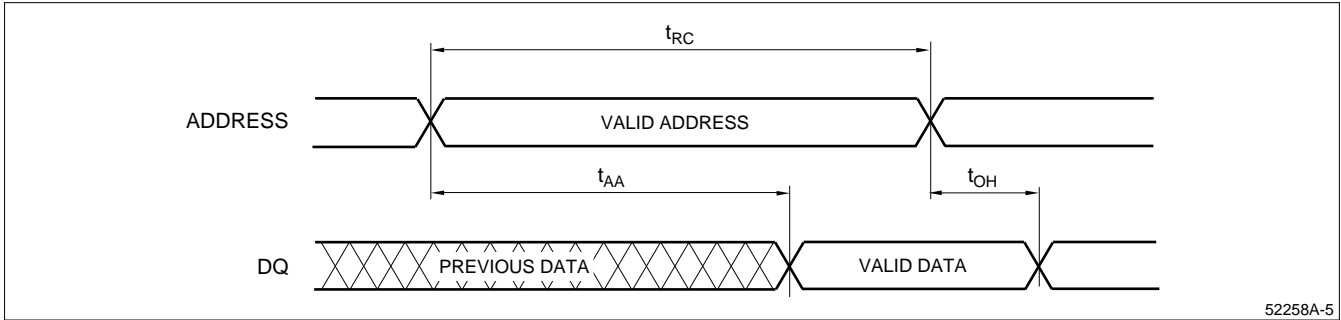
**TIMING DIAGRAMS – READ CYCLE**

**Read Cycle No. 1**

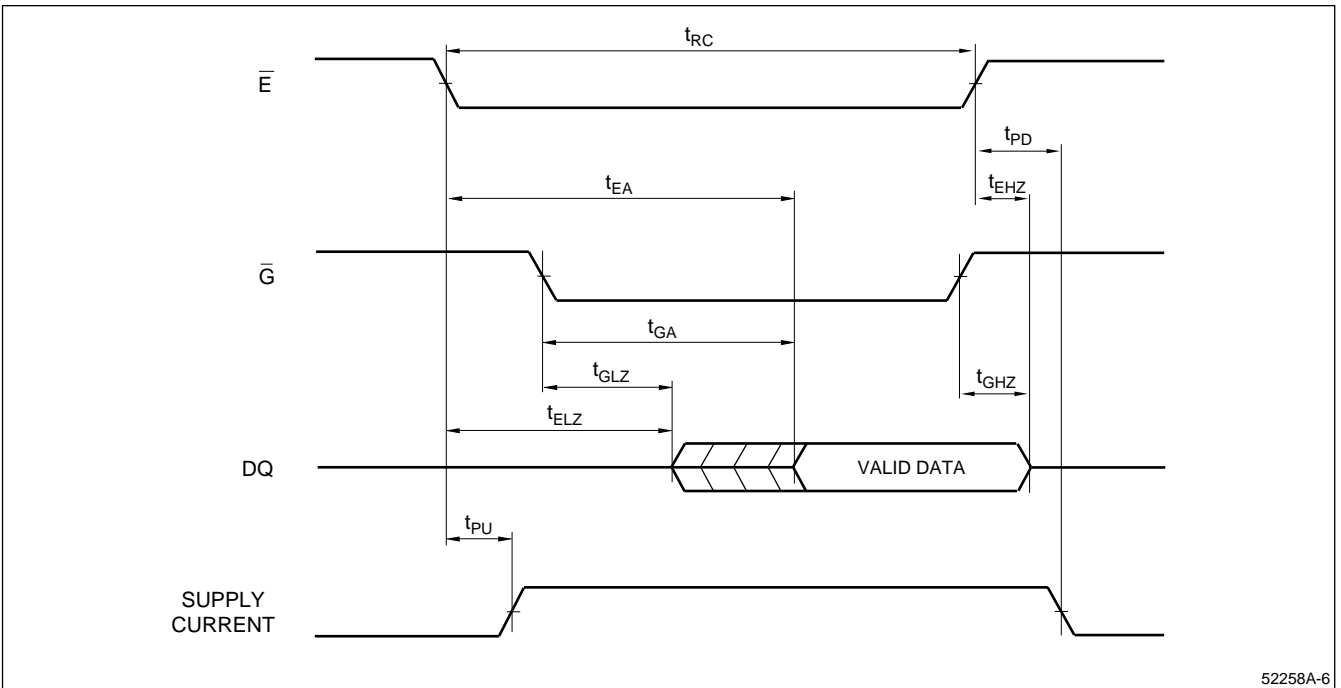
Chip is in Read Mode:  $\bar{W}$  is HIGH,  $\bar{E}$  is LOW and  $\bar{G}$  is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until  $t_{AA}$ .

**Read Cycle No. 2**

Chip is in Read Mode:  $\bar{W}$  is HIGH. Timing illustrated for the case when addresses are valid before  $\bar{E}$  goes LOW. Data Out is not specified to be valid until  $t_{EA}$  or  $t_{GA}$ , but may become valid as soon as  $t_{ELZ}$  or  $t_{GLZ}$ . Outputs will transition from High-Z to Valid Data Out. Valid data will be present following  $t_{GA}$  only if  $t_{EA}$  timing is met.



**Figure 5. Read Cycle No. 1**



**Figure 6. Read Cycle No. 2**

**TIMING DIAGRAMS – WRITE CYCLE**

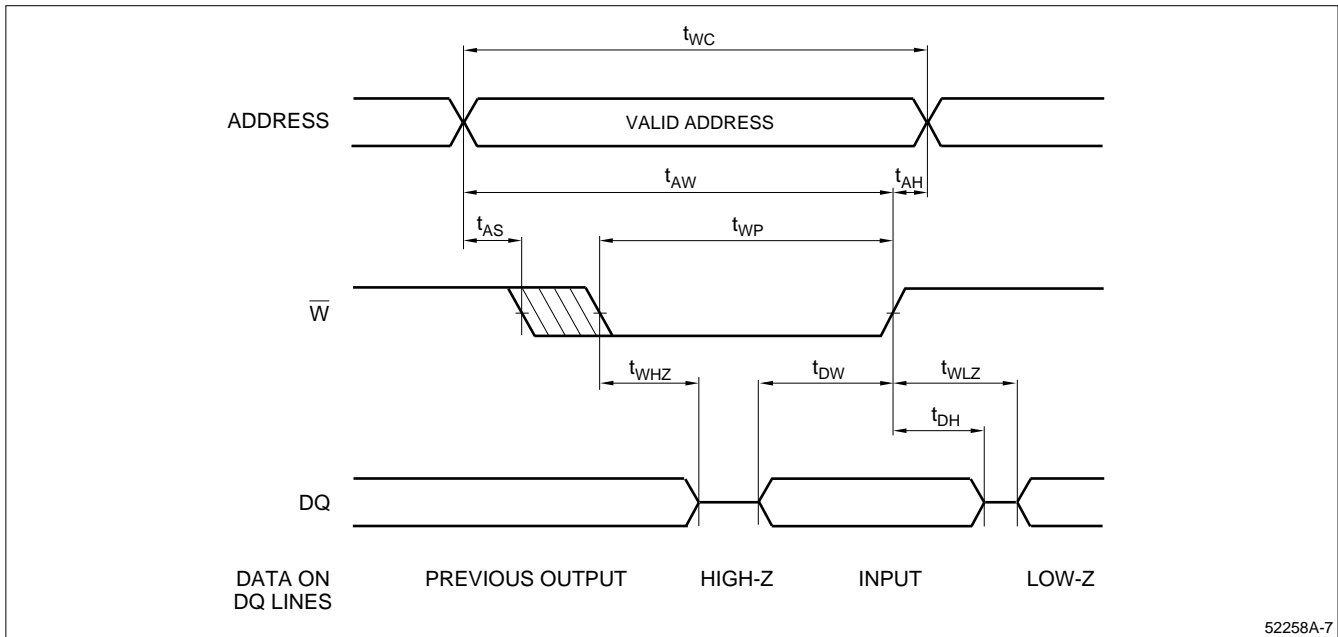
Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if  $\overline{W}$  is LOW when  $\overline{E}$  goes LOW. If  $\overline{G}$  is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with  $\overline{G}$  active, it is recommended that  $\overline{G}$  be held HIGH for all Write cycles. This will prevent the LH52258A's outputs from becoming active, preventing bus contention, thereby reducing system noise.

**Write Cycle No. 1 ( $\overline{W}$  Controlled)**

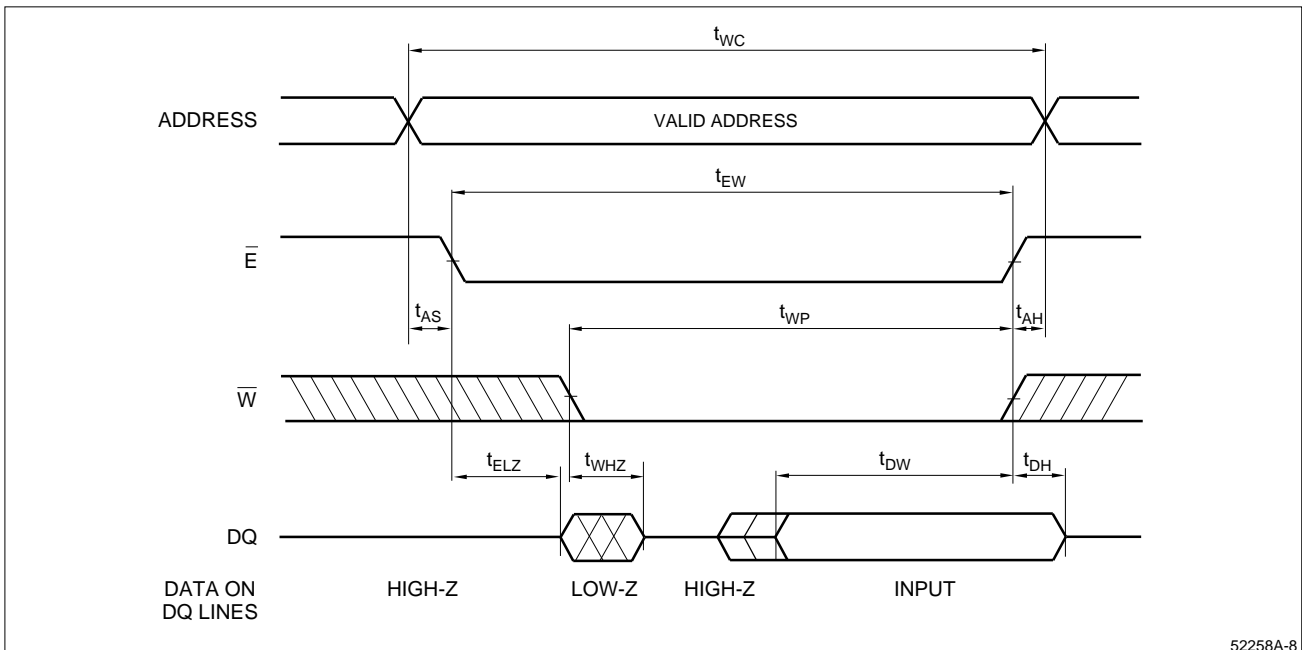
Chip is selected:  $\overline{E}$  is LOW,  $\overline{G}$  is LOW. Using only  $\overline{W}$  to control Write cycles may not offer the best performance since both  $t_{WHZ}$  and  $t_{DW}$  timing specifications must be met.

**Write Cycle No. 2 ( $\overline{E}$  Controlled)**

$\overline{G}$  is LOW. DQ lines may transition to Low-Z if the falling edge of  $\overline{W}$  occurs after the falling edge of  $\overline{E}$ .

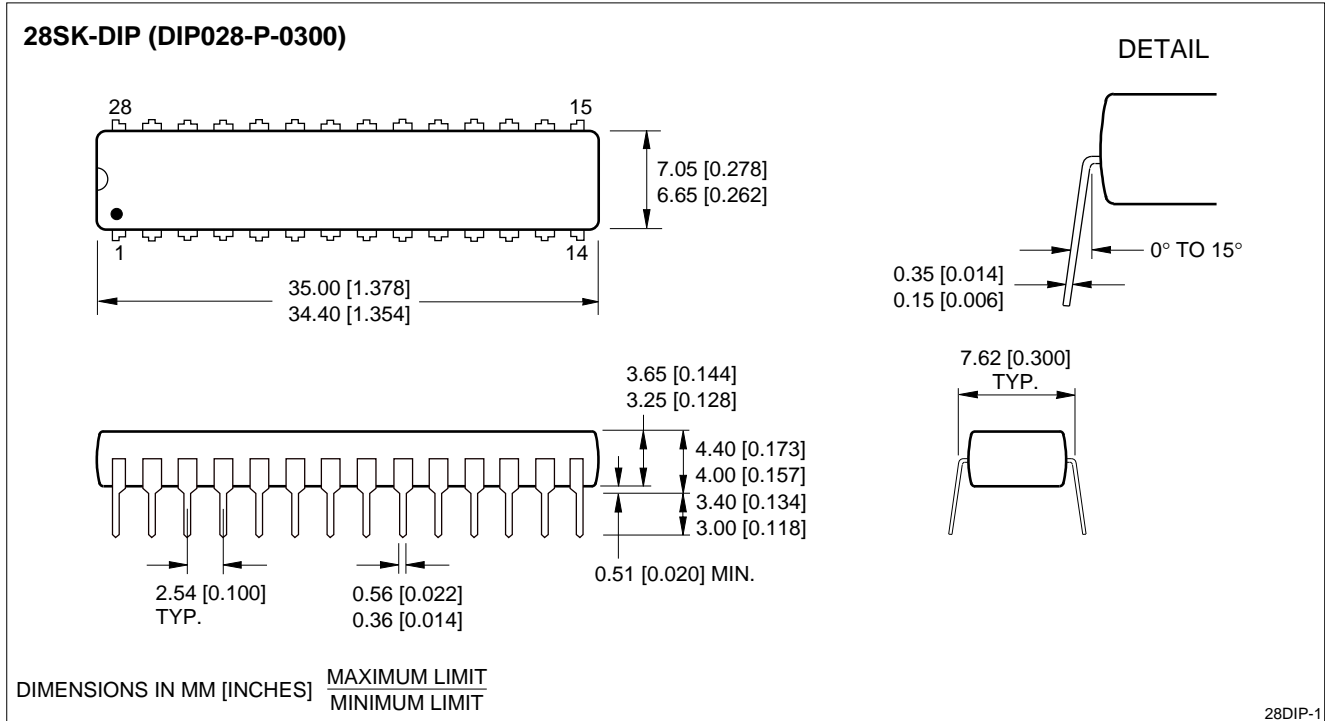


**Figure 7. Write Cycle No. 1**

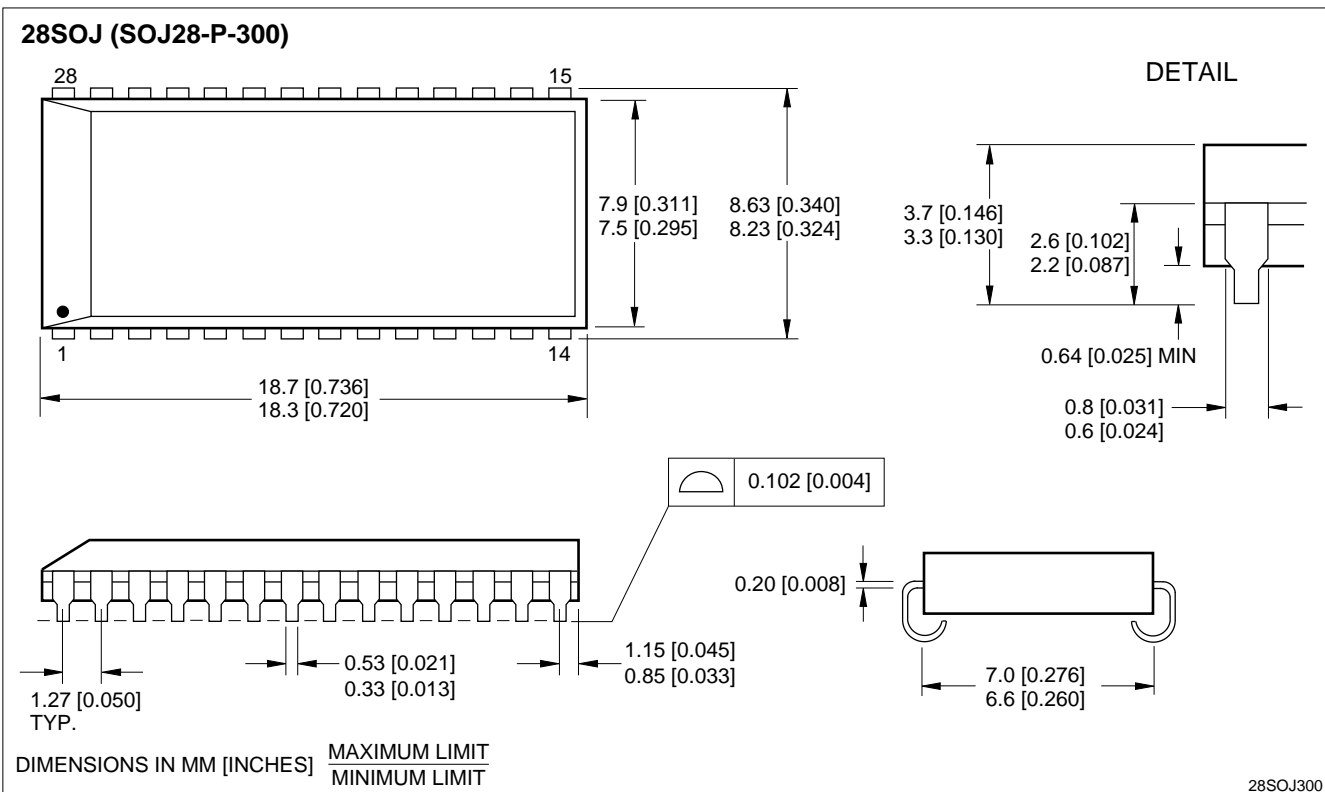


**Figure 8. Write Cycle No. 2**

PACKAGE DIAGRAMS



28-pin, 300-mil DIP



28-pin, 300-mil SOJ



## ORDERING INFORMATION

